REMARKS

Prior to examination on the merits, please amend the above-identified patent application as indicated herein. Specifically, please amend claims 167 and 168 and add claims 178-209 as indicated in attached Appendix A. Of course, claims 151-177 were previously allowed.

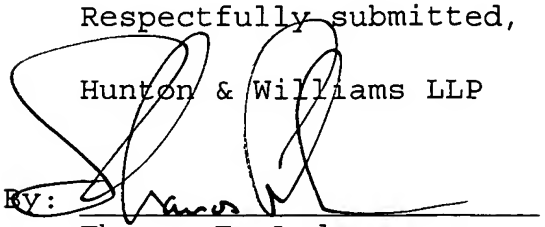
CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

Hunton & Williams LLP



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APPENDIX A

151 (Previously Presented). A memory device, comprising:

an array of dynamic random access memory cells;

a clock receiver to receive an external clock signal;

a register to store a value; and

a plurality of input receivers that includes input receivers to sample operation codes synchronously with respect to the external clock signal,

wherein a first operation code of the operation codes instructs the memory device to store the value in the register,

wherein a second operation code of the operation codes instructs the memory device to perform a write operation,

wherein, in response to the second operation code, the memory device samples write data corresponding to the write operation at a time determined using the value stored in the register, and

wherein the write data is stored in the array after being sampled.

152 (Previously Presented). The memory device of claim 151, wherein the write data is sampled by the plurality of input receivers.

153 (Previously Presented). The memory device of claim 152, wherein at least a portion of the write data is sampled by the input receivers of the plurality of input receivers that are also used to sample operation codes.

154 (Previously Presented). The memory device of claim 152, wherein the memory device includes pads coupled to the plurality of input receivers, the pads to interface with signal lines external to the memory device, wherein, for a pad from which write data is sampled, the memory device samples two bits of write data from the pad during a clock cycle of the external clock signal.

155 (Previously Presented). The memory device of claim 152, wherein the memory device includes pads coupled to the plurality of input receivers, the pads to interface with signal lines external to the memory device, wherein, for each pad from which write data is sampled, the memory device samples two bits of write data from the pad during a clock cycle of the external clock signal.

156 (Previously Presented). The memory device of claim 151, wherein the write data is stored in the array at a location

corresponding to address information, wherein the address information is sampled by the memory device synchronously with respect to the external clock signal.

157 (Previously Presented). The memory device of claim 156, wherein at least a portion of the address information is sampled by the plurality of input receivers.

158 (Previously Presented). The memory device of claim 151, wherein the value stored in the register is also used in determining a time at which read data corresponding to a read operation is output by the memory device, wherein the read data is read from the array, and wherein a third operation code of the operation codes instructs the memory device to perform the read operation.

159 (Previously Presented). The memory device of claim 158, wherein a difference between a time after which the memory device outputs the read data based on storage of a first value in the register and a time after which the memory device outputs the read data based on storage of a second value in the register is a whole number of clock cycles.

160 (Previously Presented). The memory device of claim 159, wherein the time after which the memory device outputs the read data relative to the sampling of the third operation code is about the same as the time after which the memory device samples the write data relative to the sampling of the second operation code.

161 (Previously Presented). The memory device of claim 151, wherein a difference between the time after which the memory device samples the write data based on storage of a first value in the register and the time after which the memory device samples the write data based on storage of a second value in the register is a whole number of clock cycles.

162 (Previously Presented). The memory device of claim 151, wherein the operation codes are included in request packets.

163 (Previously Presented). A memory device, comprising:

an array of dynamic random access memory cells;

a clock receiver to receive an external clock signal;

a clock generation circuit coupled to the clock receiver, the clock generation circuit to generate an internal clock signal using the external clock signal, the clock generation

circuit including:

a delay circuit to delay the external clock signal by a variable delay to produce a delayed clock signal; and

a comparison circuit, coupled to the delay circuit, to adjust the variable delay based on a comparison between the delayed clock signal and the external clock signal;

a register to store a value;

a plurality of input receivers that includes input receivers to sample operation codes synchronously with respect to the external clock signal, wherein a first operation code instructs the memory device to store the value in the register, and wherein a second operation code instructs the memory device to perform a write operation, wherein, in response to the second operation code, the memory device samples an amount of write data corresponding to the write operation at a time determined using the value stored in the register, wherein the amount of write data sampled is determined using a block size value received by the memory device, wherein the write data is sampled synchronously with respect to the external clock signal, and wherein the write data is stored in the array after being sampled;

pads coupled to the plurality of input receivers, the pads to interface with signal lines external to the memory device,

wherein, for each pad from which write data is sampled, the memory device samples two bits of write data from the pad during a clock cycle of the external clock signal; and

a plurality of output drivers coupled to the clock generation circuit, wherein the memory device outputs read data using the plurality of output drivers during a read operation, wherein the read operation is specified by a third operation code, and wherein the memory device outputs read data using the internal clock signal.

164 (Previously Presented). The memory device of claim 163, wherein the pads are located on one side of a die on which the memory device is formed.

165 (Previously Presented). The memory device of claim 163, wherein each output driver of the plurality of output drivers is coupled to a respective pad of the pads.

166 (Previously Presented). The memory device of claim 163, wherein the delay circuit includes a variable delay line and a fixed delay component.

167 (Currently Amended). The memory device of claim 163, further

including sense amplifiers, coupled to the array, to sense the read data, wherein the third operation code includes precharge information that indicates whether the sense amplifiers are to be precharged after the read data is sensed by the sense amplifiers and before a subsequent access.

168 (Currently Amended). The memory device of claim 163, wherein the write data is stored in the array ~~at a location corresponding to~~ based on address information, wherein the address information is sampled by the memory device synchronously with respect to the external clock signal.

169 (Previously Presented). The memory device of claim 168, wherein at least a portion of the address information is sampled by the plurality of input receivers.

170 (Previously Presented). The memory device of claim 163, wherein the value is received by the plurality of input receivers.

171 (Previously Presented). A method of operating a memory device, comprising:

receiving a first external clock signal;

generating an internal clock signal using the first external clock signal, wherein generating includes:

delaying the first external clock signal by a variable delay to produce a delayed clock signal;

comparing the delayed clock signal and the first external clock signal; and

adjusting the variable delay based on the comparison between the delayed clock signal and the first external clock signal;

receiving a value;

storing the value in a register on the memory device;

receiving a block size value that indicates an amount of data to be sampled during a write operation;

receiving a first operation code that indicates the write operation;

in response to the first operation code and after a write latency determined using the value stored in the register, sampling write data, wherein for a pad on the memory device from which write data is sampled, two bits of write data are sampled from the pad during a clock cycle of the first external clock signal;

storing the write data in an array of dynamic random access memory cells on the memory device;

receiving a second operation code that indicates a read operation, wherein the second operation code includes precharge information that indicates that the memory device should precharge sense amplifiers on the memory device;

in response to the second operation code and after a read latency determined using the value stored in the register, outputting read data in response to the second operation code, wherein the read data is output using the internal clock signal; and

precharging sense amplifiers on the memory device in response to the precharge information included in the second operation code.

172 (Previously Presented). The method of claim 171, wherein sampling write data further comprises sampling, from each pad on the memory device from which write data is sampled, two bits of write data during a clock cycle of the first external clock signal.

173 (Previously Presented). The method of claim 171, further comprising receiving a third operation code, and wherein storing the value in the register further comprises storing the value in the register in response to the third operation code.

174 (Previously Presented). The method of claim 173, further comprising receiving address information, wherein storing the write data further comprises storing the write data in a location of the array based on the address information.

175 (Previously Presented). The method of claim 173, wherein generating the internal clock signal further comprises:

receiving a second external clock signal; and

generating the internal clock signal using the first and second external clock signals.

176 (Previously Presented). The method of claim 175, wherein generating the internal clock signal further comprises generating the internal clock signal such that transitions of the internal clock signal occur about midway between corresponding transitions of the first and second external clock signals.

177 (Previously Presented). A method of operating a memory device, comprising:

receiving an external clock signal;

generating an internal clock signal using the external

clock signal, wherein generating includes:

delaying the external clock signal by a variable delay to produce a delayed clock signal;

comparing the delayed clock signal and the external clock signal; and

adjusting the variable delay based on the comparison between the delayed clock signal and the external clock signal;

receiving a value;

storing the value in a register on the memory device;

receiving a block size value that indicates an amount of data to be sampled during a write operation;

receiving a first operation code that indicates the write operation;

in response to the first operation code and after a write latency determined using the value stored in the register, sampling write data, wherein for each pad on the memory device from which write data is sampled, two bits of write data are sampled from the pad during a clock cycle of the external clock signal;

storing the write data in an array of dynamic random access memory cells on the memory device;

receiving a second operation code that indicates a read operation, wherein the second operation code includes precharge

information;

in response to the second operation code and after a read latency determined using the value stored in the register, outputting read data in response to the second operation code, wherein the read data is output using the internal clock signal;

if the precharge information included in the second operation code indicates that a precharge function should be performed, precharging sense amplifiers on the memory device in response to the precharge information included in the second operation code; and

if the precharge information included in the second operation code indicates that a precharge function should not be performed, holding data sensed in the sense amplifiers on the memory device.

178 (New). The memory device of claim 163, wherein, for each pad from which write data is sampled, the memory device samples four bits of write data from the pad during a clock cycle of the external clock signal.

179 (New). The memory device of claim 178, wherein the memory device includes four input receivers for each pad from which data is sampled.

180 (New). A method of operating a memory device, comprising:

receiving a first external clock signal;

generating an internal clock signal using the first external clock signal, wherein generating includes:

delaying the first external clock signal by a variable delay to produce a delayed clock signal;

comparing the delayed clock signal and the first external clock signal; and

adjusting the variable delay based on the comparison between the delayed clock signal and the first external clock signal;

receiving a value;

storing the value in a register on the memory device;

receiving a block size value that indicates an amount of write data to be sampled during a write operation;

receiving a first operation code that indicates the write operation;

in response to the first operation code and after a first amount of time determined using the value stored in the register, sampling write data, wherein for a pad on the memory device from which write data is sampled, two bits of write data

are sampled from the pad during a clock cycle of the first external clock signal;

storing the write data in an array of dynamic random access memory cells on the memory device;

receiving a second operation code that indicates a read operation, wherein the second operation code includes precharge information that indicates that the memory device should precharge sense amplifiers on the memory device;

in response to the second operation code and after a second amount of time determined using the value stored in the register, outputting read data in response to the second operation code, wherein the read data is output using the internal clock signal; and

precharging sense amplifiers on the memory device in response to the precharge information included in the second operation code.

181 (New). The method of claim 180, wherein sampling write data further comprises sampling, from each pad on the memory device from which write data is sampled, two bits of write data during a clock cycle of the first external clock signal.

182 (New). The method of claim 180, wherein sampling write

data further comprises sampling, from each pad on the memory device from which write data is sampled, four bits of write data during a clock cycle of the first external clock signal.

183 (New). The method of claim 180, further comprising receiving a third operation code, wherein storing the value in the register includes storing the value in the register in response to the third operation code.

184 (New). The method of claim 180, further comprising receiving address information, wherein storing the write data includes storing the write data in the array based on the address information.

185 (New). The method of claim 184, wherein the write data is stored in a single row within the array.

186 (New). The method of claim 180, wherein generating the internal clock signal further comprises:

receiving a second external clock signal; and

generating the internal clock signal using the first and second external clock signals.

187 (New). The method of claim 186, wherein generating the internal clock signal further comprises generating the internal clock signal such that transitions of the internal clock signal occur about midway between corresponding transitions of the first and second external clock signals.

188 (New). The method of claim 180, wherein the first amount of time and the second amount of time are about equal.

189 (New). A method of operating a memory device, comprising:

receiving an external clock signal;

generating an internal clock signal using the external clock signal, wherein generating includes:

delaying the external clock signal by a variable delay to produce a delayed clock signal;

comparing the delayed clock signal and the external clock signal; and

adjusting the variable delay based on the comparison between the delayed clock signal and the external clock signal;

receiving a value;

storing the value in a register on the memory device;

receiving a block size value that indicates an amount of

write data to be sampled during a write operation;

receiving a first operation code that indicates the write operation;

in response to the first operation code and after a first amount of time determined using the value stored in the register, sampling the amount of write data, wherein for a pad on the memory device from which write data is sampled, two bits of write data are sampled from the pad during a clock cycle of the external clock signal;

storing the amount of write data in an array of dynamic random access memory cells on the memory device;

receiving a second operation code that indicates a read operation, wherein the second operation code includes precharge information that indicates whether the memory device should precharge sense amplifiers on the memory device after read data is sensed in the sense amplifiers and before a subsequent access;

in response to the second operation code and after a second amount of time determined using the value stored in the register, outputting the read data in response to the second operation code, wherein the read data is output using the internal clock signal;

when the precharge information included in the second

operation code indicates that the memory device should precharge the sense amplifiers, precharging the sense amplifiers on the memory device in response to the precharge information included in the second operation code; and

when the precharge information included in the second operation code indicates that the memory device should not precharge the sense amplifiers, holding data sensed in the sense amplifiers on the memory device.

190 (New). The method of claim 189, wherein sampling write data further comprises sampling, from each pad on the memory device from which write data is sampled, two bits of write data during a clock cycle of the first external clock signal.

191 (New). The method of claim 189, wherein sampling write data further comprises sampling, from each pad on the memory device from which write data is sampled, four bits of write data during a clock cycle of the first external clock signal.

192 (New). The method of claim 189, further comprising receiving a third operation code, wherein storing the value in the register includes storing the value in the register in response to the third operation code.

193 (New). The method of claim 189, further comprising receiving address information, wherein storing the write data includes storing the write data in the array based on the address information.

194 (New). The method of claim 193, wherein the write data is stored in a single row within the array.

195 (New). A dynamic random access memory device having an array of memory cells, comprising:

a clock generation circuit to generate an internal clock signal, the clock generation circuit including:

a delay circuit to delay an input signal by a variable delay to produce a delayed signal; and

a comparison circuit, coupled to the delay circuit, to adjust the variable delay based on a comparison between the delayed signal and the input signal;

a register;

a plurality of input receivers that includes input receivers to sample input signals to produce sets of bits corresponding to control information, wherein a first set of bits instructs the memory device to store a value in the

register, and wherein a second set of bits instructs the memory device to perform a write operation during which the memory device samples an amount of write data at a time determined using the value stored in the register, wherein the amount of write data sampled is determined using a block size value received by the memory device, wherein the amount of write data is stored in the array;

pads coupled to the plurality of input receivers, the pads to interface with signal lines external to the memory device, wherein, for each pad from which write data is sampled, the memory device samples two bits of write data from the pad during a clock cycle of the internal clock signal; and

a plurality of output drivers coupled to the clock generation circuit, wherein the memory device outputs read data using the plurality of output drivers during a read operation, wherein the read operation is specified by a third set of bits, and wherein the memory device outputs read data using the internal clock signal.

196 (New). The memory device of claim 195, further including sense amplifiers, coupled to the array, to sense the read data, wherein the third set of bits includes a bit that indicates whether the sense amplifiers are to be precharged after the read

data is sensed by the sense amplifiers and before a subsequent access.

197 (New). The memory device of claim 195, wherein, for each pad from which write data is sampled, the memory device samples four bits of write data from the pad during a clock cycle of the internal clock signal.

198 (New). A dynamic random access memory device, comprising:

an array of dynamic random access memory cells, wherein write data is written to the array in response to a first set of bits that specifies a write operation;

a register to store a value, wherein the value is written to the register in response to a second set of bits, wherein the value is used to determine when the write data is to be sampled by the memory device, wherein an amount of write data to be written to the array is specified by block size information received by the memory device; and

a plurality of input receivers that includes input receivers to sample input signals to produce sets of bits corresponding to control information, wherein the first and second sets of bits are included in the sets of bits.

199 (New). The memory device of claim 198, wherein one bit of each set of bits indicates that the set of bits specifies one of a read operation and a write operation.

200 (New). The memory device of claim 198, further comprising:

a plurality of output drivers to output read data during a read operation, wherein the read operation is specified by a third set of bits, wherein the read data is output onto a set of external signal lines as a part of the read operation and the write data is input from the same set of external signal lines as a part of the write operation.

201 (New). The memory device of claim 200, further including sense amplifiers, coupled to the array, to sense the read data, wherein the third set of bits includes a bit that indicates whether the sense amplifiers are to be precharged after the read data is sensed by the sense amplifiers and before a subsequent access.

202 (New). A system, comprising:

a memory controller; and

a plurality of memory devices coupled to the memory controller, wherein a first memory device of the plurality of memory devices includes:

an array of dynamic random access memory cells, wherein write data is written to the array in response to a first set of bits that specifies a write operation, wherein the write data is received from the memory controller;

a register to store a value that is received from the memory controller, wherein the value is written to the register in response to a second set of bits, wherein the value is used to determine when the write data is to be sampled by the first memory device, wherein an amount of write data to be written to the array is specified by block size information provided by the memory controller to the first memory device; and

a plurality of input receivers that includes input receivers to sample input signals received from the memory controller to produce sets of bits corresponding to control information, the sets of bits including the first and second sets of bits.

203 (New). The system of claim 202, wherein one bit of each set of bits indicates that the set of bits specifies one of a read operation and a write operation.

204 (New). The system of claim 202, wherein the first memory device further comprises:

a plurality of output drivers to output read data to the memory controller during a read operation, wherein the read operation is specified by a third set of bits, wherein the read data is output by the first memory device onto a set of external signal lines as a part of the read operation and the write data is input by the first memory device from the same set of external signal lines as a part of the write operation.

205 (New). The system of claim 204, wherein the first memory device includes sense amplifiers, coupled to the array, to sense the read data, wherein the third set of bits includes a bit that indicates whether the sense amplifiers are to be precharged after the read data is sensed by the sense amplifiers and before a subsequent access.

206 (New). The system of claim 202, wherein the memory controller selects one of the first memory device and a second memory device of the plurality of memory devices to respond to a third set of bits that specifies that the selected memory device perform a write operation, wherein the memory controller selects

the selected memory device using additional bits sent with the third set of bits.

207 (New). The system of claim 206, wherein the additional bits correspond to a device identifier that selects one of the first and second memory devices.

208 (New). The system of claim 206, wherein the additional bits correspond to an address range.

209 (New). The system of claim 206, wherein the additional bits are included in a packet with the third set of bits.